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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/932,680	08/20/2001	Chrong-Jung Lin	TS1998-850/852B	5633

28112 7590 07/28/2003

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EXAMINER
PIZARRO CRESPO, MARCOS D

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 07/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/932,680	LIN ET AL.	
	Examiner	Art Unit	
	Marcos D. Pizarro-Crespo	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *29 and 32-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *29 and 32-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Attorney's Docket Number: TS1998-850/852B
Filing Date: 8/20/2001
Claimed Priority Date: 11/1/1999 (Divisional 09/431,236)
Applicant(s): Lin et al.
Examiner: Marcos D. Pizarro-Crespo

DETAILED ACTION

This Office action responds to the amendment in paper no. 13 filed on 6/26/2003.

Acknowledgment

1. The amendment in paper no. 13, filed on 6/26/2003, in response to the Office action in paper no. 12, mailed on 3/24/2003, has been entered. The present Office action is made with all the suggested amendments being fully considered. Accordingly, pending in this Office action are claims 29 and 32-40.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 29, 32-34, and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (US 5482881), Hsu (US 5854108), and Taketa (US 5939749).

5. Regarding claim 29, Chen shows (see, *e.g.*, figs. 8-9) most aspects of the instant invention including a stacked-gate memory-cell pair having a graded doubly diffused drain (DDD) profile comprising:

- a semiconductor substrate **116** of a first conductivity type having active and passive regions defined and having a top surface
- a pair of stacked gates overlying the substrate surface, each stacked gate having:
  - a gate oxide layer **120** overlying the substrate **116**
  - a floating gate layer **122** overlying the gate oxide layer **120**
  - an inter-gate oxide layer **124** overlying the floating gate **122**
  - a control gate **126** overlying the inter-gate layer **124**
- diffusion regions **114** of a second conductivity type formed within the substrate **116** and adjacent to each of the stacked gates
- a common diffusion region **112** of a second conductivity type formed within the substrate **116** and defined between the pair of stacked gates

- channel regions **118** within the substrate **116** lying beneath the pair of stacked gates and defined between the diffusion regions **114** and the common drain region **112**
- a heavily-doped implanted region **132** within the common drain region **112**
- a lightly-doped implanted region **130** beneath and surrounding the heavily-doped implanted region **132**

wherein the lightly-doped and the heavily-doped implanted regions are smoothly graded doping profiles that extend from the common diffusion region toward the center of the channel region (see, *e.g.*, fig. 9), and wherein the smoothly graded doping profiles are defined by a tilt-angle impurity-implantation (see, *e.g.*, figs. 8D and 8E).

Chen, however, fails to show sidewall spacers conforming to the stacked-gates. On the other hand, Hsu (see, *e.g.*, abstract) teaches that these sidewall spacers may enhance the overall memory-cell pair performance.

Accordingly, it would have been obvious at the time of the invention to one of ordinary skill in the art to include sidewall spacers as part of Chen's memory-cell pair, as suggested by Hsu, to increase the overall performance of the device.

Finally, it should be noted that although Chen refers to the common diffusion region as "a source region" (see, *e.g.*, col.10/ll.8) and to the diffusion regions adjacent to the stacked gates as "drain regions" (see, *e.g.*, col.8/ll.13), the identification of these electrodes could be reversed, given alternative voltage levels in the device. That is to say, the electrode labels of 'drain' and 'source' are interchangeable depending upon the

voltage levels. On this topic, Taketa teaches a good example on the interchangeability between source and drain regions (see, *e.g.*, Taketa col.5/ll.1-8 and col.12/ll.40-50).

Consequently, as taught by Taketa, it would have been obvious at the time of the invention to one of ordinary skill in the art that the drain and source labels in the semiconductor device of Chen/Hsu may be interchanged depending on the voltage levels applied to the device.

6. Regarding claim 32, Chen shows that the lightly doped implanted region comprises phosphorous ions at a dosage level between about $1x10^{13}$ to $5x10^{13}$ atoms/cm^2 (see, *e.g.*, fig. 4F).

7. Regarding claim 33, Chen shows that the heavily doped implanted region comprises arsenic ions at a dosage level between about $1x10^{15}$ to $5x10^{15}$ atoms/cm^2 (see, *e.g.*, fig. 7).

8. Regarding claim 34, the limitations referring to the operational characteristics of the memory-cell pair must result in a structural difference between the claimed memory-cell pair and that of the prior art in order to patentably distinguish the claimed invention. If the prior art structure is capable of performing the intended use, then it meets the claim. *In re Casey*, 152 USPQ 235 (CCPA 1967); *In re Otto*, 136 USPQ 458, 459 (CCPA 1963). In the instant case, operating the claimed pair with a minimal disturb voltage difference of about $|0.18V|$ does not appear to result in any structural differences between the claimed memory-cell pair and that of the prior art.

9. Regarding claim 40, Chen shows that the impurity-implantation tilt-angle is between about 40 to 50 degrees from the horizontal (see, *e.g.*, col.9/ll.57-67).

10. Claims 35 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen in view of Taketa, Hsu, and Maiti (US 5861347).

11. Regarding claim 35, Chen/Taketa/Hsu shows most aspects of the instant invention (see paragraphs 5-9 above). They, however, fail to specify the thickness of the gate oxide layer. Maiti, on the other hand, teaches that a typical thickness for this layer falls between 80 and 95Å (see, *e.g.*, Maiti col.4/ll.46-48).

Accordingly, it would have been obvious at the time of the invention to one of ordinary skill in the art that the gate oxide of Chen/Hsu/Taketa was between 80 and 95Å thick, as taught by Maiti, since these thicknesses are typically used in the semiconductor art for gate oxide layers.

12. Regarding claim 37, Chen/Taketa/Hsu shows most aspects of the instant invention (see paragraphs 5-9 above). They, however, fail to specify the thickness of the inter-gate oxide layer. Maiti, on the other hand, teaches that a typical thickness for this layer falls between 120 and 160 Å (see, *e.g.*, Maiti col.5/ll.9-22).

Accordingly, it would have been obvious at the time of the invention to one of ordinary skill in the art that the inter-gate oxide of Chen/Taketa/Hsu was between 120 and 160 Å thick, as taught by Maiti, since these thicknesses are typically used in the semiconductor art for inter-gate oxide layers.

13. Claims 36 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen in view of Taketa, Hsu, and Hong (US 5445984).

14. Regarding claim 36, Chen/Taketa/Hsu shows most aspects of the instant invention (see paragraphs 5-9 above). They, however, fail to specify the thickness of

the floating gate. Hong, on the other hand, teaches that a typical thickness for this gate falls between 1000 and 2000 Å (see, *e.g.*, Hong col.4/ll.64-68).

Accordingly, it would have been obvious at the time of the invention to one of ordinary skill in the art that the floating gate layer of Chen/Taketa/Hsu was between 1000 and 2000 Å thick, as taught by Hong, since these thicknesses are typically used in the semiconductor art for floating gates.

15. Regarding claim 38, Chen/Taketa/Hsu shows most aspects of the instant invention (see paragraphs 5-9 above). They, however, fail to specify the thickness of the control gate. Hong, on the other hand, teaches that a typical thickness for this gate falls between 1500 and 2000 Å (see, *e.g.*, Hong col.7/ll.41).

Accordingly, it would have been obvious at the time of the invention to one of ordinary skill in the art that the control gate of Chen/Taketa/Hsu was between 1500 and 2000 Å thick, as taught by Hong, since these thicknesses are typically used in the semiconductor art for control gates.

16. Claim 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen in view of Taketa, Hsu, and Lin (US 5501997).

17. Regarding claim 39, Chen/Taketa/Hsu shows most aspects of the instant invention (see paragraphs 5-9 above). They, however, fail to specify the thickness of the sidewall spacers. Lin, on the other hand, teaches that a typical thickness for these spacers falls between 1200 and 1500 Å (see, *e.g.*, Lin col.2/ll.61).

Accordingly, it would have been obvious at the time of the invention to one of ordinary skill in the art that the sidewall spacers of Chen/Taketa/Hsu were between

1200 and 1500 Å thick, as taught by Lin, since these thicknesses are typically used in the semiconductor art for sidewall spacers.

Response to Arguments

18. Applicant's arguments with respect to claims 29 and 32-40 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

19. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

20. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

21. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. Papers should be faxed to Art Unit 2814 via the Art Unit 2814 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November

1989). The Art Unit 2814 Fax Center number is **(703) 308-7722** or **–7724**. The Art Unit 2814 Fax Center is to be used only for papers related to Art Unit 2814 applications.

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Marcos D. Pizarro-Crespo** at **(703) 308-6558** and between the hours of 9:30 AM to 8:00 PM (Eastern Standard Time) Monday through Thursday or by e-mail via Marcos.Pizarro@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy, can be reached on (703) 308-4918.

23. Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 308-0956**.

24. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass(es): **257**/314-326,336,344,345,408 **438**/163,257-267	3/12/2003
Other Documentation: PLUS Analysis	5/25/2002
Electronic Database(s): EAST (USPAT, EPO, JPO)	3/12/2003

SUPERVISORY PRIMARY EXAMINER
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MDP/mdp
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